

Remarks

Thorough examination by the Examiner is noted and appreciated.

No new matter has been added.

For example support for the amendments is found, for example in Figure 4 and in the Specification:

beginning at the second paragraph on page 7:

"For advanced semiconductor technology, precise temperature control is of utmost importance since unintended variations in process temperatures may result in excessive oxide growth on the substrate, among other considerations.

Critical dimension (CD) shifts occur at a rate of over 1 nm (nanometer) per degree Celcius change in reaction temperature, and within-wafer CD shifts as great as 3 nm have been known due to process temperature variations. As device features become smaller and smaller, these unintended process temperature variations become increasingly problematic. Conventional temperature control methods and systems are capable of controlling unintended shifts in ESC temperatures to within about 5 degrees Celsius. **Accordingly, a system and method is needed which is capable of controlling ESC temperature shifts to within 0.5 degrees Celsius."**

beginning at the second paragraph on page 13:

"A main circulation loop 67 of the temperature control system 54 includes a main coolant delivery line 62 that confluently connects the main coolant chamber 58 of the chiller 56 to the ESC 52 of the reaction chamber 42,

typically through a delivery line valve 70, which may be a solenoid valve. The main coolant delivery line 62 is disposed in fluid communication with a network of main coolant channels 82 which are **distributed throughout the ESC 52 for substantially uniformly imparting a temperature** of the main coolant 59 to the ESC 52 as the main coolant 59 flows through the main coolant channels 82, as hereinafter further described."

**Claim Rejections under 35 USC 102**

1. Claims 1, 9, and 15 stand rejected under 35 USC Section 102(b) as being anticipated by (Laid Open Kokai Patent JP9-17770-A), herein after referred to as Akira et al. to correspond with Examiners designation; however, inventor is Fukuda Seiichi).

Akira et al. disclose a method for maintaining a substrate at a uniform temperature by circulating a lower temperature coolant to a substrate support peripheral portion (item 11, Figure/Example 1) compared to a higher temperature coolant circulated at a central portion of the substrate support (see item 14). Akira et al. overcome the problem of preferential heating of a wafer at the peripheral portions by radiant heat from the walls of a heated plasma chamber (see page 3,

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[constitution], claim 1, paragraphs 0006, 0011, 0019, 0028, 0029, 0032; Figure 2).

Thus, the method and apparatus of Akira et al. works by a **different principal of operation** than Applicants method. Akira et al **keeps a wafer at a set point temperature** by differentially cooling the substrate support while Applicants **keep a substrate support at a setpoint temperature**.

Akira et al. does not disclose:

"A method of maintaining a substrate support at a **substantially uniform set point temperature** in a reaction chamber upon a rise in temperature of the chamber"

Thus, Akira et al. is insufficient to anticipate Applicants disclosed and claimed invention.

#### **Claim Rejections under 35 USC 103**

2. Claims 2, 4, 6, 8, 10, and 12 stand rejected under 35 USC

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Section 103(a) as being unpatentable over Akira et al. above.

Applicants reiterate the comments made above with respect to Akira et al.

Examiner argument that the set point temperature is an optimizable parameter is inapplicable where the general conditions of Applicants disclosed and claimed invention have not been shown in the prior art. As noted above, the method of Akira et al. works by a different principle of operation than Applicants and the method of Akira et al. accomplishes the opposite result from Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

3. Claims 3 and 5 stand rejected under 35 USC Section 103(a) as being unpatentable over Akira et al. above and further in view of Okudaira et al. (5,705,029).

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Applicants reiterate the comments made above with respect to Akira et al.

Even assuming *arguendo*, proper motivation to combine the teachings of Akira et al. and Okudaira et al., the fact that Okudaira et al. tech **maintaining the temperature of an etched article** over a range of temperatures during the etching process by changing pressure and/or wafer temperature (by a cooling stage provided with a single coolant temperature) (see Abstract; Figure 7) (e.g., where the wafer is between 50 to 130 deg C during etching (see col 6, lines 33-37; lines 50-59), does not further help Examiner in producing Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

4. Claims 7, 11, and 16 stand rejected under 35 USC Section 103(a) as being unpatentable over Akira et al. above and further in view of Hideo et al. (JP 2003-248322 also published as US PUB 2004033435).

Applicants reiterate the comments made above with respect to Akira et al.

Even assuming *arguendo*, proper motivation to combine the teachings of Akira et al. and Hideo et al., the fact that Hideo et al. teach blowing cold air onto a support to maintain a temperature support (where the cold air is at temperature of less than 50 C) in a printing plate process (see paragraph 0146-0148, does not further help Examiner in producing Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck*, 947

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*F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

5. Claims 13,14, and 17-20 stand rejected under 35 USC Section 103(a) as being unpatentable over Akira et al. above and further in view of Long et al. (US 6,608,352).

Applicants reiterate the comments made above with respect to Akira et al.

Even assuming *arguendo* a proper motivation for combining Akira et al. with Long et al., the fact the Long teaches forming test PN junctions and heating the PN junctions to a plurality of temperatures while applying a bias Voltage and passing a current through the PN junctions to create current versus temperature characteristics of the PN junctions and then using those current versus temperature characteristics to determine the temperature resistance of a field effect transistor by measuring the current of an actual PN junction while the filed effect transistor is dissipating different level of power, (see e.g., Abstract), does not further help Examiner in producing Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when

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combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

### **Conclusion**

The cited references, either singly or in combination, fail to produce Applicants disclosed and claimed invention and therefore fail to make out a *prima facie* case of anticipation or obviousness.

Applicants have amended the independent claims to further clarify Applicants invention.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in

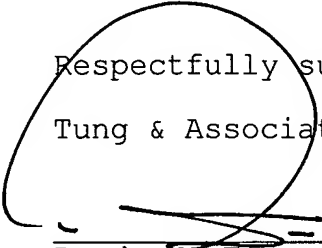


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a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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